Version of Substitute Specification With Markings to Show Changes

Electronic Timepiece With Checking Function, And Its Checking Method Therefor

Inventors: Shinji Nakamiya
Katsuyoshi Takahashi

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to an electronic timepiece ~~operating by the power supply of~~ powered by a ~~charge~~rechargeable battery, and to a checking method for the timepiece.

Description of the Related Art

[0002] There ~~are~~ exists a variety of portable electronic timepieces such as wristwatches and ~~electrical~~ electric clocks. Some of these timepieces have ~~chargeable~~a rechargeable power source such as ~~chargeable~~rechargeable batteries or large-capacitance capacitors. ~~And in s~~Some others have removable~~,~~ battery units ~~are constructed as removable unit~~. In ~~these~~ timepieces, time-keeping units and digital (or analog) displaying units for displaying time ~~conduct operation~~ operate by using ~~the electrical~~ electric power stored ~~on~~ in the~~ batteries~~ power source.

[0003] FIG. 11 ~~shows~~is a flowchart showing ~~one~~ an example of a manufacturing process and a checking process for a timepiece with a battery and a charging means for the battery.

[0004] ~~As for~~ In FIG. 11, discharging step~~ (step~~ A101~~)~~ is ~~done~~ conducted before the remaining steps in the manufacturing process of the ~~electrical~~electric timepiece.

[0005] In ~~this~~ discharging step A101, by ~~using~~ use of an external discharging circuit, ~~for example as~~ such as that shown in FIG. 12, the battery alone is discharged~~ alone~~. In the external discharging circuit 100 shown in FIG. 12, a plurality of~~ (n piece of)~~ batteries (i.e. n batteries) from BA1 to BAn are placed on a battery ~~placing~~ mounting section 101. Each battery from BA1 to BAn is connected in series to a resister from R1 to Rn, respectively. A sink type constant voltage power source 102 is connected in parallel to each of the above series-connected resisters and batteries. ~~By~~ In the above-configured external discharging circuit 100, batteries ~~from~~ BA1 to BAn are discharged at the same time. In this case, the number of installation terminals for the batteries in the external discharging circuit

100 ~~have~~ has to be enough for the number of batteries to be discharged at the same time.

[0006] After ~~this~~ battery discharging step ~~(step~~ A101~~)~~, an assembling step ~~(step~~ A102~~)~~ and an exterior installation step ~~(step~~ A103~~)~~ ~~is~~ are conducted. Then a battery charging step ~~(step~~ A104~~)~~ is conducted.

[0007] In this charging step A104, the quality of the charging function of the battery is examined, and enough ~~electrical~~ electric energy for ~~the electrical timepiece~~ operation ~~in~~ of the next step ~~of~~ (i.e. an operation checking ~~step~~ (step A105) is stored in the battery. Charging is conducted in the following ways. ~~For example, for~~ In a timepiece ~~with~~ having a rotating type generator, ~~giving a vibration to~~ causing the timepiece to vibrate moves an oscillation weight in the rotating-type generator of the timepiece, and~~. A~~ kinetic energy ~~generated~~ in the oscillation weight ~~in this process~~ is converted by the generator into ~~electrical~~ electric energy, ~~and then the electrical energy~~ which is subsequently stored in the battery. ~~And in other type of~~ In a timepiece ~~such as with~~ having a solar panel, electric energy is generated~~ion is conducted~~ by the solar panel, and the generated ~~electrical~~ electric energy is stored in the battery. ~~And~~ In yet ~~in~~ another type of timepiece, it is possible to generate electric energy from ~~use for generation~~ an inductive energy source, ~~in accordance with~~ such as an exterior radio wave or a magnetic force, and to thereby charge the battery.

[0008] Confirmation of a charging state is conducted ~~in the following way~~as follows. ~~In~~ in the charging step, an operator ~~puts~~ activates a charging state display function ~~into action, the charging state display function being~~ that is installed in the timepiece. ~~And the~~ The operator then checks the display~~ing state of the timepiece, and~~ to confirms whether ~~or not the charging~~ the battery is ~~over~~chargedd.

[0009] ~~The b~~Battery discharging step ~~(step~~ A101~~)~~ ~~mentioned above is done in order~~ is implemented to~~, at this charging step, control an~~ maintain the accuracy of the monitoring of battery voltage ~~inspection~~ in the charging step to within a certain range.

[0010] In ~~the~~ operation checking step ~~(step~~ A105~~)~~, ~~a~~ quality verification for the ~~electrical~~ electric timepiece is conducted. This quality verification comprises timepiece operation verification ~~in~~ at high and ~~cold~~ low temperatures. ~~In detail~~Specifically, in the operation checking step, a trial operation lasting several hours or several tens of hours is conducted at ~~around~~ an ambient temperature of about 60 degree centigrade ~~of high temperature atmosphere~~ and ~~around~~ at an ambient temperature of about minus 10 degree centigrade ~~of low temperature atmosphere, a trial operation extending several hours or several tens of hours is~~

~~conducted~~. ~~In~~ During this trial operation period, the timepiece is checked for ~~a~~ stoppage and for a delay ~~of~~ in displayed time ~~display is checked~~. ~~And~~ Then, by confirming a continuous discharging time of the battery after the trial operation, ~~a~~ quality confirmation (judgment) is conducted.

[0011] After ~~the~~ operation checking step A105, a shipment checking ~~step (~~step A106~~)~~, ~~with~~ including an exterior check~~ing~~, and a full-charging step ~~(step~~ A107~~)~~ to ~~full~~ fully charge the battery ~~is~~ are conducted, and then the timepiece is shipped (step A108).

[0012] ~~Incidentally~~It is to be noted, in the battery discharging step explained above, ~~discharging~~ the battery ~~is conducted~~ alone is discharged by using the external discharging circuit before ~~the assembling~~assembly~~.~~, ~~And~~ and that discharging ~~time requires~~ the battery requires from several to several tens of hours. Therefore, a discharging circuit facility ~~with~~ requires enough ~~number of, for example enough for one day production of timepiece,~~ battery installation terminals ~~for the batteries is necessary~~ for one day's production. Hence, this discharging method is not appropriate for a model produced on a massive scale.

[0013] ~~And~~ Also if, for example, after the shipment, a~~n operation~~ verification operation ~~for~~ of a discharging function is required, it is very difficult for the battery to be ~~made on a certain discharging state~~ discharged to a predetermined level without a discharging facility.

[0014] Moreover, there are several kinds of ~~battery~~ batteries. Even among lithium type ~~battery~~ batteries, discharging characteristics differs, for example, according to types of electrodes, as shown in FIG. 13. ~~And chargeable~~Also, rechargeable batteries ~~battery has~~ have a characteristic of voltage recovery effect by which, after ~~stopping~~ discharging is stopped, voltage rises. Therefore battery voltage is unstable and becomes ~~wide~~ dispersed after discharging. This voltage dispersion after discharging ~~causes a disadvantageous effect~~ adversely affects ~~on~~ the accuracy of checking ~~accuracy~~.

[0015] ~~And~~ Furthermore by purchasing a certain switch while in the charging step~~,~~ ~~for example~~, a charging state, such as charged~~ing~~ voltage, is ~~displayed~~ indicated by ~~the~~ an amount of fast-forwarding movement of the analog second hand on the displaying section~~, by pushing a certain switch~~. In this case, an external operation such as pushing a certain switch or the like is necessary to ~~confirm~~ determine the charging state. Hence an external input is required, ~~and~~ resulting in a problem of necessitating a further ~~more~~ operation process. ~~And~~ Also, since ~~confirmation is done by~~ a use confirms a charging state by observing the amount of fast-forwarding movement of the analog second hand, ~~if the amount of fast-forwarding movement is~~

~~wrongly recognized~~, there is a possibility ~~that checking result falls in a fault judgment~~ of misjudgment due to human error.

[0016] ~~And~~ Additionally in the operation checking step, ~~the~~ quality verification ~~for~~ of the ~~electrical~~ electric timepiece is conducted by checking ~~the~~ its operation ~~under~~ at both ~~a~~ high and low ambient temperatures ~~atmosphere~~. More precisely, quality verification of the timepiece is conducted by checking whether ~~or not~~ the time piece experiences ~~there is~~ a stoppage (continuous time-keeping trouble) or a time delay under the above conditions~~, the quality verification of the timepiece is conducted~~. Therefore even when ~~the trouble~~ a problem is detected in the timepiece, it is difficult to ~~identify~~ determine whether the cause of the ~~trouble~~ problem ~~whether it~~ is due to the motor drive unit or due to the battery.

[0017] ~~In order to~~ To confirm that ~~it~~ a problem is due to ~~a~~ motor drive trouble, it is ~~required~~ necessary to examine ~~even~~ a gear train unit ~~for~~ that drives ~~driving~~ an hour hand, a minute hand and a second hand. ~~And in order to do~~ To conduct this examination, it is ~~required~~ necessary to dismantle ~~break~~ the timepiece ~~up by~~ to a considerabl~~ey~~ extent requiring fine detail. Hence, in order to ~~prevent~~ avoid this complicated ~~breaking up work and~~ dismantling examination procedure, there is a demand for simplifying the distinction ~~that distinction~~ between a problem due to ~~the~~ motor drive trouble and a problem due to another factor ~~be made as easy as possible~~. However, in the prior art~~s timepiece~~, it is difficult to ~~make a distinction~~ distinguish between ~~the~~ a motor drive ~~trouble~~ problem and a problem due to another factor.

[0018] ~~And as for the~~ Regarding motor drive trouble, ~~as long as the~~ when a motor ~~is~~ does not ~~apparently~~ appear to be of ~~low~~ poor quality, it is not possible to judge that the trouble is due to the motor. ~~But~~However, for example, there ~~is somewhat~~ exist some low quality motors which, under some temperature conditions, work~~s~~ ~~and does not~~ without causinge a delay. Ideally, ~~this kind of~~ such motors should also be judged ~~as~~ to cause motor problems. However it is difficult to make such a ~~judgement~~judgment.

[0019] ~~By t~~Taking the above situation into ~~considering~~ consideration, the object of the present invention is to provide an ~~electrical~~ electric timepiece with a checking function which, for example, in the timepiece manufacturing process ~~enhances~~ improves ~~the~~ checking accuracy and efficiency, and a checking method for the timepiece.

Objects of the Invention

[0020] Therefore, it is an object of the present invention to overcome the aforementioned problems.

Summary of the Invention

[0021] ~~In order to~~ To solve the above problems, in the timepiece of the present invention~~, a timepiece~~ comprises an external input unit for receiving an external signal, a display section for displaying the time, a battery unit capable of being recharged~~ing~~, a drive unit for driving the display section ~~by~~ using the ~~electrical~~ electric power stored in the battery unit, a comparator unit, and a discharging control unit. The comparator unit ~~detects a~~ monitors the voltage of the battery unit, and compares the voltage with a reference voltage. The discharging control unit, when~~, via the external input terminal,~~ a prescribed signal ~~enters~~ is input via the external input terminal, starts discharging ~~from~~ the battery unit, and when the ~~detected result by the~~ comparator unit ~~satisfies~~ detects a prescribed condition, stops ~~the~~ discharging ~~from~~ the battery unit.

[0022] ~~By the~~ The present invention~~, it is possible to~~ provides the following advantages:~~.~~ ~~Being able to check the~~ timepiece operation ~~more accurately and efficiently~~ can be checked with improved accuracy and efficiency;~~.~~ ~~Unnecessity of~~ an external circuit for discharging the battery in the manufacturing process is unnecessary; and~~.~~ ~~Being able to lower~~ the voltage dispersion of the battery can be lowered before and after ~~and before~~ charging.

Brief Description of the Drawings

[0023] FIG. 1 is a block diagram showing a construction of ~~the~~ a timepiece of one embodiment of the present invention.

[0024] FIG. 2 is a flowchart showing a ~~flow~~ process of manufacturing and checking ~~process of~~ the timepiece.

[0025] FIG. 3 is a block diagram showing constructions of each part of the timepiece.

[0026] FIG. 4 is a circuit diagram showing the construction of the operation check function control circuit 310 shown in FIG. 3.

[0027] FIG. 5 is a circuit diagram showing a second external input unit measure circuit 311, operation check function mode select circuit 312, a stored electricity unit discharge control circuit 305, a stored electricity unit charging completion detect circuit 306, and a motor drive trouble detect circuit 304 shown in FIG. 3.

[0028] FIGS. 6A and 6B are timing charts showing operation of the operation check function control circuit 310 shown in FIG. 3.

[0029] FIG. 7 is an exemplary operational timing chart ~~showing one example of operations~~ of ~~each unit~~ the structure shown in FIG. 3.

[0030] FIG. 8 is a block ~~chart~~ diagram explaining a discharging current in a motor drive unit E shown in FIG. 3.

[0031] FIGS. 9A, 9B and 9C ~~cooperate to~~ collectively form a flowchart showing flow of operation and checking process of the timepiece of the present invention.

[0032] FIG. 10 is ~~a diagram showing a specification of the operation and checking~~ a diagram explaining modes 1 to 3 of the operation check process.

[0033] FIG. 11 is a flowchart showing an operation and checking process of ~~the~~ a timepiece ~~of~~ according to prior art~~s~~.

[0034] FIG. 12 is a circuit showing an external discharging circuit for batteries ~~of~~ according to prior art~~s for batteries~~.

[0035] FIG. 13 is a diagram showing discharging characteristics of two types of lithium ~~chargeable~~ rechargeable battery (MT: which uses manganese and titanium for electrode, CT: which uses titanium and carbon for electrode).

Description of the Preferred Embodiments

[0036] ~~From here, by using~~ With reference to the drawings, one embodiment of present invention will be described. FIG. 1 is a block diagram which shows a construction of the timepiece 1 of one embodiment of the present invention. In FIG. 1, the timepiece 1 is a wristwatch. ~~User of this wristwatch wears it by using a belt attached to the apparatus.~~ The ~~electrical~~ electric timepiece 1 comprises a generator system A, a power supply system B, a control unit C, a motor unit D, a motor drive circuit E, a first external input terminal F, and a second external input terminal G. ~~Brief~~ A brief explanation~~s~~ of ~~these parts are as~~ the operation of these components follows. The generator system A generates alternating current. The power supply system B rectifies the alternating current, then stores the generated energy into the battery unit 48, and then raises or lowers the stored voltage, and then supplies ~~the electricity to each constructing parts~~ power to the electrically driven components. The control unit C controls the entire timepiece 1. The motor unit D comprises a second hand 61, a minute hand 62, a hour hand 63, and a stepping motor 10 for moving the hands. The motor drive circuit E is a circuit for driving the stepping motor 10 in the motor unit D, based on a control signal from the control unit C. The first external input unit F and the second external input unit G are means for

changing modes in an operation check~~ing~~ ~~mode~~ process~~ in turn~~. This operation check ~~function~~ process is one feature of the timepiece 1 of the present invention.

[0037] The generator system A comprises a generating apparatus 40, an oscillating weight 45, and an acceleration gear 46. The generating apparatus 40 in FIG. 1 is an electromagnetic induction type AC generator apparatus. The electromagnetic induction type AC generator apparatus comprises a generator rotor 43, a generator stator 42, and a generator coil 44. The oscillating weight 45 is a means for providing the generator rotor 43 with ~~an~~ energy. In this wristwatch type ~~electrical~~ electric timepiece 1, the oscillating weight 45 is ~~driven~~ made to rotate by movement of a user's arm. The movement of the oscillating weight 45 is transmitted to a generator rotor 43~~,~~ via ~~the~~ an acceleration gear 46~~, is transmitted to a generator rotor 43~~. Then the generator rotor 43 rotates in a generator stator 42. ~~Then~~ thus voltage is induced in the generator coil 44. The voltage is output ~~to between~~ from two output terminals of the generator coil 44. In this way, in the generator system A, power generation is ~~done~~ achieved by use of energy related to the user's everyday life.

[0038] The power supply system B comprises a rectifier circuit 47, a battery (a battery unit) 48 and a voltage raising and lowering circuit 49. The alternating voltage from the generator system A is rectified by the rectifier circuit 47 into a direct voltage, and is stored in the battery (the battery unit) 48. The battery unit 48 comprises a large-capacitance capacitor or a ~~chargeable~~rechargeable battery such as a lithium battery. The direct voltage stored in the battery 48 is supplied to the voltage raising and lowering circuit 49. The voltage raising and lowering circuit 49 is a circuit for, by using more than one of capacitors ~~of from~~ 49a to 49c, raising or lowering the direct voltage by multiple~~ times~~ factors. The output voltage of the voltage raising and lowering circuit 49 is controllable by a control signal ϕ11 from the control unit C.

[0039] In the structure shown in FIG. 1, ~~a voltage VDD of~~ higher electric potential side of ~~the~~ battery 48 ~~(higher electric potential side voltage)~~ is ~~described~~ identified as a reference electric potential GND. ~~And a~~ The lower electric potential side ~~voltage~~ of ~~the~~ battery 48 is ~~described~~ identified as a first voltage low reference VTKN~~ (a first lower electric potential side voltage)~~,~~.~~ ~~And~~ and a second voltage on the lower electric potential side ~~voltage~~ of ~~the~~ raising and lowering circuit 49 is ~~described~~ identified as a second ~~lower electric potential side~~ voltage low reference VSS. Output voltage of ~~the~~ generator coil 44 is input to ~~the~~ control unit C as a control signal ϕ13. ~~A voltage value of v~~Voltage VSS is input to the control unit C as a control signal ϕ12.

[0040] A motor drive circuit E creates a drive pulse based on a drive clock supplied from ~~the~~ control unit C, and then provides the drive pulse to a stepping motor 10 in ~~the~~ motor unit D. ~~The s~~Stepping motor 10 comprises a rotator section. The rotator section rotates by a fixed ~~degree~~ amount when ~~the~~ a drive pulse is ~~supplied~~ applied to ~~the~~ stepping motor 10. The rotation of the rotating part of ~~the~~ stepping motor 10 is transmitted to ~~the~~ second hand 61 by way of a second intermediate wheel 51 and a second wheel 52, both wheels being connected to the rotating part. ~~Then t~~The second hand thus rotates providing an indication of the passage of time in seconds~~,~~ ~~and the second indication is conducted~~. ~~And~~ Additionally, the rotation of the second wheel 52 is transmitted to a minute intermediate wheel 53, a minute wheel 54, an hour intermediate wheel 55, and an hour wheel 56. The minute wheel 54 is connected to a minute hand 62. The hour wheel 56 is connected to a hour hand 63. Therefore these hands works ~~together~~ in conjunction with the rotation of ~~the~~ stepping motor 10,~~. And~~ and thereby indicate the passage of time in hours and minutes~~ indications are conducted~~.

[0041] Although not described in the drawings, it is possible to connect other transmission systems to the gear train 50 which is constructed ~~by~~ of wheels ~~from~~ 51 to 56 in order to display a calendar and so on. For example, ~~in order~~ to display a date, it is possible to ~~put~~ add a cylindrical intermediate wheel, an intermediate date wheel, and a date wheel and so on. ~~And~~ Further still, it is possible to ~~put~~ add a calendar correction gear train (such as a first calendar correction wheel, a second calendar correction wheel, a calendar correction wheel, and a date disc).

[0042] The first external input unit F comprises a crown for setting time ~~setting~~ and a circuit for electrically detecting the time-setting operation~~ electrically~~. In this embodiment, the second external input unit G is used as a switch for starting ~~the~~ an operation check function of the timepiece 1~~ has~~. The second external input terminal G is an indicator switch installed on the exterior section of the wristwatch. The second external input terminal G is used ~~when confirming~~ to confirm the charging state of ~~the~~ battery 48. ~~And also~~ Also in this embodiment, the second external input terminal G is used as a switch for inputting a signal to change between modes ~~of from~~ 1 to 3 while ~~operating~~ performing the operation check process (B100). Operation state of the first external input unit F and the second external input unit G is input to the control unit C in ~~electrical~~ the form of an electric signal.

[0043] ~~Here, by referring~~ With reference to FIG. 2, an outline of the operation check process ~~realized in~~ of this embodiment will be described. FIG. 2 is a flowchart showing an example of a manufacturing and checking process of the ~~electrical~~ electric timepiece of the present embodiment. The operation check process B100 is

conducted after the manufacturing process (step A102) and the exterior installation process (step A103). The operation check process B100 ~~is composed of~~ has three ~~processes~~ steps (step B101, step B104, and step B105). These three ~~processes is~~ steps are conducted by using ~~each~~ functions of modes ~~from~~ 1 to 3 which ~~the~~ are present in the timepiece ~~has in itself~~.

[0044] The first process (step B101) of the operation check process B100 ~~is corresponding~~ corresponds to discharging step A101 in FIG. 11. The first process is ~~conducted~~ executed as a preparation ~~process~~ step for checking the charging function of ~~the~~ timepiece 1. In ~~the~~ this first process, ~~by~~ use of mode 2 ~~function~~ of ~~the~~ timepiece 1, starts an ~~electrical~~ electric power consumption circuit ~~is put to start~~, ~~and the electrical power consumption circuit~~ which discharges ~~electrical~~ electric charge ~~stored in the~~ from battery 48~~,~~ and thereby controllably drops the voltage of the battery ~~is controlled into a~~ to prescribed voltage level.

[0045] The second process step (step B104) of the operation check process B100 is a process for ~~judging~~ determining the efficiency, or ~~a~~ quality, of a charging ~~performance~~operation. This~~e~~ second process is ~~conducted~~ implemented by a charging-performance-quality-judge function of mode 2 ~~function~~ of ~~the~~ timepiece 1 ~~(charging performance quality judge function)~~. ~~In more details,~~ More specifically in this second process, the ~~electrical~~ electric timepiece 1 is supplied with a vibration, and ~~thereby the~~ its internal oscillating weight ~~in it is driven to~~ is thereby made to rotate. ~~Therefore~~ Thus, electricity is generated in ~~the~~ generator system A, and ~~charging the~~ battery 48 is ~~done~~ charged. Then, the charging-performance-quality-judge function ~~by the~~ of mode 2 ~~function (charging performance quality judge function),~~ determines if ~~whether or not~~ the battery's voltage reaches a ~~charging completion~~ charge-complete voltage level within a prescribed ~~charging~~ period of time~~is judged~~, and the result ~~of judgement~~ is ~~displayed~~ conveyed to the user by movement of second hand 61. That is, mode 2 determines if the battery is charged up to a predetermined voltage level within a prescribed time period, and outputs the result.

[0046] The third process (step B105) of the operation check process B100 is a process for poor quality detection by operating the timepiece 1. In more detail~~s~~, in this third process, ~~under~~ at high or low temperatures ~~condition~~, although motor drive circuit E is ~~being~~ able to rotate ~~the~~ stepping motor 10, drive circuit E generates an irregular motor drive pulse, which will result in ~~more electrical~~ higher electric power consumption ~~is generated from the motor drive circuit E~~. Operation ~~under this kind of~~ at these severe conditions enable~~s to~~ detection of motor ~~characteristic~~ trouble, which is not ~~possible to~~ detectable ~~under~~ when generating a

normal motor drive pulse. When ~~the~~ trouble is detected, movement of, for example, ~~the~~ second hand 61 is changed from a normal state to ~~other~~ a different state, ~~and~~ which ~~the~~ state is ~~continued~~ maintained. The user sees that the movement of second hand is different ~~from~~ than in the normal state, and thereby knows that there is a problem with the motor ~~characteristics has some trouble~~.

[0047] Next, ~~by using~~with reference to FIGS. 3 to 8, details of each ~~construction~~ part of ~~the~~ timepiece 1 shown in FIG. 1 will be described. FIG. 3 is a block diagram showing detail of the construction of the control unit C, and signal flows between units of from A to G. In FIG. 3, blocks of from 301 to 312 are circuit blocks in the control unit C, and those surrounded by ~~broken~~ dashed lines are not.

[0048] The charge detecting circuit 301 receives the output voltage of ~~the~~ generator coil 44 as a generation voltage signal SW (ϕ13), and, ~~by~~ in accordance with the signal, detects a generation state of the generator system A. ~~And t~~Then the circuit 301 outputs ~~the result showing~~ a signal indicating a detection result of the charging state as a charge detect result signal SA. ~~The s~~Signal SA which ~~enters into~~ is input to ~~the~~ rectifier circuit 47 in ~~the~~ power supply system B is used as a signal for controlling a rectification operation. The ~~R~~rectified output of ~~the~~ rectifier circuit 47 is supplied to ~~the~~ battery 48 (the battery unit) ~~48~~ as a rectification output signal SB. ~~And a~~ A stored voltage signal SC showing the stored voltage (=VKTN) of battery 48 ~~enters~~ is applied to ~~into~~ a raising and lowering circuit 49 and a voltage detecting circuit 302.

[0049] The voltage detecting circuit 302 receives the stored voltage signal SC, a stored voltage raising and lowering result signal SD (ϕ12=VSS), and a voltage detect control signal SX. The stored voltage raising and lowering result signal SD is a signal indicating the output voltage of the raising and lowering circuit 49. The voltage detect control signal SX is output from a timepiece control circuit 303. The voltage detecting circuit 302, when the voltage detect control signal SX is active, compares the signal SC, which ~~of~~ indicat~~ing~~es the stored voltage VKTN, with predetermined reference comparison voltages of DCHRGV and CHRGV respectively, then outputs a voltage detect result signal SN comprised of bits SN1 and SN2 indicating respective comparison results.

[0050] ~~Incidentally~~It is to be noted that~~,~~ ~~other~~ rather than ~~direct comparison between the~~ comparing stored voltage VTKN ~~and~~ with the reference comparison voltages, it is possible to compare~~s, instead of the stored voltage VTKN,~~ the raising and lowering voltage VSS with the reference voltages ~~of DCHRGV and CHRGV, and then~~and to output~~s~~ the ~~voltage detect~~ comparison result as signal SN.

[0051] For example, when the raising and lowering circuit 49 is ~~on a state of raising ratio of~~ operated to provide a raising factor of 2, if it is detected that the absolute value of VSS is 1.25 V ~~is detected~~, outputting the voltage detect result signal SN indicating the absolute value of VTKN of 0.625 V gives an equivalent effect.

[0052] The timepiece control circuit 303 uses the output voltage VSS of the raising and lowering circuit 49 as a power source. The timepiece control circuit 303 receives a first and a second stored electricity unit discharge control signals SO1 and SO2 from a stored electricity unit discharge control circuit 305, a stored electricity unit charge completion control signal SP from a stored electricity unit charging completion judge circuit 306, a motor drive trouble judge signal SQ from a motor drive trouble judge circuit 304, a high-frequency magnetic field detect result signal SK from high-frequency magnetic field detect circuit 307, an alternating current magnetic field detect result signal SL from an alternating current magnetic field detect circuit 308, and a rotation detect result signal SM from a rotation detect circuit 309.

[0053] Then the timepiece control circuit 303 generates the voltage detect control signal SX, and supplies it to the voltage detecting circuit 302.

[0054] ~~And t~~The timepiece control circuit 303 generates ~~a~~ motor driving signals SE, SF, SG, and SH, and supplies them to the motor drive circuit E, and also generates a non-rotation detect measure signal SY, and supplies it to the motor drive trouble judge circuit 304.

[0055] The motor drive signal SE is a pulse signal comprised of a normal driving pulse, a rotation detect pulse, a high frequency magnetic field detect pulse, a magnetic field detect pulse, ~~and~~ an auxiliary pulse, and so on. The normal driving pulse is a pulse supplied to the motor drive circuit E for a regular motor drive. The rotation detect pulse is a pulse supplied to the motor drive circuit E when detecting whether ~~or not~~ there is a high-frequency magnetic field. The high frequency magnetic field detect pulse is a pulse supplied to the motor drive circuit E for detecting an external magnetic field. The auxiliary pulse is a pulse that is output when the motor fails to rotate ~~by~~ in response to only the normal driving pulse. This auxiliary pulse~~, and~~ has ~~bigger~~ higher effective electric power than the normal driving pulse. When the auxiliary pulse is generated, the non-rotation detect measure signal SY is generated.

[0056] The motor driving signal SF is a pulse for controlling the motor driving circuit E when discharging the battery 48.

[0057] The motor driving signal SG is a pulse for controlling the motor unit D when charging ~~the~~ of battery 48 is completed.

[0058] The motor driving signal SH is a pulse for controlling the motor unit D ~~to~~ for ~~other~~ hand movement ~~from~~ other than normal hand movement, and~~,~~ is output when motor trouble takes place~~, is output~~.

[0059] When a high-frequency magnetic field detect pulse is supplied to the motor drive circuit E as the motor drive signal SE, a bidirectional induced voltage is generated in a drive coil of the stepping motor. The high frequency magnetic field detect circuit 307 is a circuit ~~to~~ detecting existence of a high-frequency magnetic field by comparing a voltage SJ of the induced voltage with the pre-determined reference value for alternating current magnetic field detection.

[0060] When a magnetic field detect pulse is supplied to the motor drive circuit E as the motor drive signal SE, a bidirectional induced voltage is generated in a drive coil of the stepping motor. The alternating current magnetic field detect circuit 308 is a circuit ~~to~~ for detecting existence of an alternating current magnetic field by comparing a voltage SJ of the induced voltage with the pre-determined reference value for alternating current magnetic field detection.

[0061] When a rotation detect pulse is supplied to the motor drive circuit E as the motor drive signal SE, a bidirectional induced voltage is generated in a drive coil of the stepping motor. The rotation detect circuit 309 is a circuit ~~to~~ for detecting existence of a rotation of the drive motor by comparing a voltage SJ of the induced voltage with the pre-determined reference value for rotation detection.

[0062] ~~Incidentally~~It is to be noted that~~,~~ a section in the timepiece control circuit 303 for outputting the motor drive signal SE, the high frequency magnetic field detect circuit 307, the alternating current magnetic field detect circuit 308, and the rotation detect circuit 309 are based on known techniques~~ which have been~~ used for controlling a stepping motor drive. For example, the technique is described in Japanese Patent Application Laid-Open Publication No.10-225191 entitled "~~c~~Control ~~d~~Device for ~~s~~Stepping ~~m~~Motor, ~~i~~Its ~~c~~Control ~~m~~Method, and ~~t~~Time ~~k~~Keeping ~~d~~Device", and Japanese Patent Publication No. 3-45798 entitled "~~a~~Analog ~~e~~Electric ~~t~~Timepiece"~~ explain the technique~~, both of which are hereby incorporated by reference.

[0063] An operation check function control circuit 310 receives a first external input signal SR1 and a first external input differential signal SR2. The first external input signal SR1 is a signal output from a first external input unit F, ~~and~~ indicating that a switch (a crown) in the first external input unit F is operated. The

first external input differential signal SR2 is a differentiated signal of the first external input signal SR1. ~~And t~~The operation check function control circuit 310 outputs an operation check function control signal SS.

[0064] A second external input unit measure circuit 311 receives an operation check function control signal SS and a second external input signal ST. The second external input signal ST is a signal output from a second external input unit G, ~~and~~ indicating that a switch (a crown) in the second external input unit G is operated. ~~And t~~The second external input unit measure circuit 311 outputs an operation check function mode select signal SU which has two bits of SU1 and SU2.

[0065] The operation check function mode select circuit 312 receives the operation check function mode select signal SU and the operation check function control signal SS. And the operation check function mode select circuit 312 outputs an operation check function mode select result signal SV which has three bits of SV1, SV2, and SV3. The three bits of SV1, SV2, and SV3 of the operation check function mode select result signal SV ~~enters into~~ are input to the stored electricity unit discharge control circuit 305, the stored electricity unit charging completion judge circuit 306, and the motor drive trouble judge circuit 304 respectively. A bit SV1 of the operation check function mode select result signal SV is a bit indicating by positive logic that the operation check function is in the mode 1. The bit SV1 ~~has the~~ is at a high level when the mode of the operation check function is in the mode 1. A bit SV2 is a bit indicating by positive logic that the operation check function is in the mode 2. The bit SV2 ~~has the~~ is at a high level when the mode of the operation check function is in the mode 2. A bit SV3 is a bit indicating by negative logic that the operation check function is in the mode 3. The bit SV3 ~~has the~~ is at a low level when the mode of the operation check function is in the mode 3.

[0066] Next, referring to FIGs. 4, 5, and 7, ~~the~~ a description will be ~~given~~ provided with respect to the operation check function control circuit 310, the second external input unit measure circuit 311, the operation check function mode select circuit 312, the stored electricity unit discharge control circuit 305, the stored electricity unit charging completion judge circuit 306, and the motor drive trouble judge circuit 304.

[0067] FIG. 4 is a circuit diagram showing the detailed ~~construction of the~~ operation of check function control circuit 310 shown in FIG. 3. The operation check function control circuit 310 comprises two 2-bit counters 401 and 402, a 1-bit counter 403, two D ~~flip-flap~~flip-flops 404 and 405, an SR latch 406, three double-input ORs 407 to 409, a double-input AND 410, a double-input XNOR (exclusive logic addition of negative logic output) 411, and ~~two double-input of positive logic~~

~~input and negative logic input~~ ANDs 412 and 413 each of which has a positive logic input terminal and a negative logic input terminal.

[0068] An output signal of OR gate 408 is input to ~~In~~ the reset terminal R of the 2-bit counter 401 ~~enters an output signal of the OR 408~~. A clock signal F1 having a cycle of one second ~~In~~ is input to the clock terminal CLK of the 2-bit counter ~~401 enters a clock signal F1 having a cycle of one second~~. The 2-bit counter 401 counts the clock signal F1 when the output signal of the OR 408 ~~has the~~ is at a low level.

[0069] The first external input signal SR1 is input to ~~In~~ the positive logic input terminal of the AND 412 ~~enters the first external input signal SR1~~. The signal SR1 ~~becomes the~~ is set to a high level when the crown, which is the switch of the first external input unit F, is pulled out by two clicks.

[0070] The first external input differential signal SR2 is input to ~~In~~ the positive logic input of the AND 413 ~~enters the first external input differential signal SR2~~. The signal SR2 is a differentiated signal of the signal SR1. In more detail, the signal SR2 is generated ~~under a case~~ when the crown in a state of being pulled out by two clicks is pushed back by one click or two, the first external input signal SR1 is reset from a high level ~~turns~~ to ~~the~~ a low level ~~from the high level~~. The signal SR2 is a single pulse signal having a predetermined pulse width.

[0071] The operation check function mode select circuit 312 output the operation check function mode select result signal SV2, which is applied to ~~In~~ the negative logic input ~~of the~~ AND~~s~~ gates 412 and 413 ~~enters the operation check function mode select result signal SV2 output from the operation check function mode select circuit 312~~. When the signal SV2 ~~has the~~ is at a low level, ~~the~~ AND~~s~~ gates 412 and 413 output the first external input signal SR1 and the first external input differential signal SR2 as they are.

[0072] The clock signal F1 having a cycle of one second is input to ~~In~~ the clock terminal CLK of the 1-bit counter 403 ~~enters the clock signal F1 having a cycle of one second~~. The output of AND gate 412 is input to ~~In~~ the active low reset terminal R ~~having the low active~~ of the 1-bit counter 403 ~~enters the output signal of the AND 412~~. The 1-bit counter 403 counts pulses in ~~the~~ clock signal F1 when the output signal of ~~the~~ AND gate 412 ~~has the~~ is at a high level.

[0073] The data terminal D of ~~the~~ D ~~flip-flap~~flip-flop 404 is fixed at ~~the~~ a high level. ~~In t~~The reset terminal R ~~having the low active~~ of D ~~flip-flap~~flip-flop 404 is active low. ~~enters the~~ The output ~~signal of the~~ of AND gate 412 is applied to the reset terminal R of D flip-flop 404. Output XQ of 1-bit counter 403 is applied to ~~In~~ the clock input terminal, CLK, of ~~the~~ D ~~flip-flap~~flip-flop 404 ~~enters the output signal~~

~~of the output terminal XQ of the 1-bit counter 403~~. Accordingly, ~~under a state that the~~ when the output signal of ~~the~~ AND gate 412 ~~has the~~ is at a high level, ~~when the output signal of the output terminal XQ of the 1-bit counter rises, the D flip-flap~~D flip-flop 404 responds to a rise at output XQ of 1-bit counter 403 by ~~reads~~ latching in the ~~input signal having~~ high level at its data terminal D~~which is given to the data terminal D~~ and ~~outputs~~ outputting the same from ~~the~~ its output terminal Q.

[0074] The data terminal D of the D ~~flip-flap~~flip-flop 405 is fixed at ~~the~~ a high level. ~~In the r~~Reset terminal R ~~having the low active~~ of D ~~flip-flap~~flip-flop 405 is active low and it receives ~~enters~~ the output ~~signal of the~~ from AND 410. The output from AND aate 412 ~~In~~ is applied to the clock input terminal CLK of ~~the~~ D ~~flip-flap~~flip-flop 405~~ enters the output signal of the AND 412~~. Accordingly, when ~~under a state that~~ the output signal of ~~the~~ AND gate 410 ~~has the~~ is high~~ level~~, ~~when the output signal of the AND 412 rises, the~~ D ~~flip-flap~~flip-flop 405 will reads ~~the~~ its input high signal ~~having high level which is given to the data~~ at its terminal D and outputs the same ~~from the~~ on output terminal Q in response to a rise at the output of AND gate 412.

[0075] The OR 407 receives the "2^1 " output Q1 ~~of the~~ from 2-bit counter 401 and ~~the~~ output ~~signal from the output terminal~~ Q ~~of the~~ from D flip-flop 405.

[0076] The output OR gate 407 ~~In the~~ coupled to the set terminal S of ~~the~~ SR latch 406~~ enters the output signal of the OR 407~~. Output Q of D flip-flop 404 ~~In the~~is applied to the reset terminal R of ~~the~~ SR latch 406.~~ enters the output signal from the output terminal Q of the D flip-flap 404.~~

[0077] The OR 409 outputs ~~a logical sum~~ the logic OR function of the output ~~signal of the output terminal~~ Q of ~~the~~ SR latch 406 and ~~an~~ the output ~~signal~~ of ~~the~~ AND gate 413.

[0078] The output of OR gate 409 ~~In~~ is applied to the clock terminal CLK of ~~the~~ 2-bit counter 402~~ enters the output signal of the OR 409~~. The output Q of SR latch 406 is applied to ~~In~~ the reset terminal R of ~~the~~ 2-bit counter 402~~ enters the output signal of the output terminal Q of the SR latch 406~~. When the output of SR latch 406 is at a low level, ~~The~~ counter 402~~, when the output signal of the SR latch 406 has the low level,~~ counts ~~the~~ signal SR2 supplied via ~~the~~ AND gate 413 and OR gate 409. Here, when the output of ~~the~~ OR 407, which is ~~to be a~~ coupled to the set input S of ~~the~~ SR latch 406 ~~has the~~ is at a low level, the output Q of ~~the~~ SR latch 406 ~~becomes the low level by receiving the~~ is reset in response to a high level signal ~~once in the~~ at its reset input R.

[0079] The 2-bit counter 402 has a "2^0" output (i.e. Q0) and a "2^1" output (i.e. Q1). These output terminals are connected to input terminals of ~~the~~ AND gate 410. ~~Accordingly, in a case in which the~~ When output Q of ~~the~~ SR latch 406 ~~has the~~ is at a low level, signal SR2 is permitted to pass through OR gate 409 to 2-bit counter 402. Thus, if the output of SR latch 406 is low, ~~when as~~ and three SR2 ~~three~~ pulse signals are applied to the ~~enter into~~ the 2-bit counter 402, ~~both~~ the outputs (Q0 and Q1) of the 2-bit counter 402 will go ~~become the~~ high ~~level~~ upon the third pulse of signal SR2 and cause the output ~~signal~~ of ~~the~~ AND gate 410 to becomes ~~the~~ high ~~level~~.

[0080] The output signal of the AND 410 is output as operation check function control signal SS from the operation check function control circuit 310. The signal SS, when ~~the~~ at a high level, starts the operation check function. ~~And the s~~Signal SS is also input to the active low reset input ~~terminal~~ R ~~having the low active~~ of ~~the~~ D flip-flop 405, as mentioned above.

[0081] The XNOR 411 outputs a high level, when both of the "2^0" output Q0 and the "2^1" output Q1 of ~~the~~ counter 402 ~~have the~~ are at a low level or both are at a high level.~~, outputs a signal of high level, and~~ XNOR 411 outputs a low level when both Q0 and Q1 of counter 402 at ~~when the levels of them are~~ different levels~~, outputs a signal having the low level~~.

[0082] ~~The~~ OR gate 408 outputs a logical OR function ~~sum~~ of the output signal ~~of the~~ from XNOR 411 and the output signal ~~of the~~ from AND gate 413. The output of OR gate 408 is applied to ~~the~~ reset terminal R of ~~the~~ 2-bit counter 401.

[0083] FIG. 6A, 6B, and 7 are timing ~~charts~~ diagrams ~~showing~~ of a function of the operation check function control circuit 310 explained above.

[0084] First, ~~the state~~ when the operation check function mode is ~~not at the~~ other than mode 2, the operation check function mode select result signal SV2 ~~has the~~ is at a low level, and the operation check function control signal SS which is at a ~~has the~~ low level will be described.

[0085] In this case, the operation check function control circuit 310 receives the signal SR1 ~~having the~~ which is at a high level for more than 1 or 2 seconds (period T1) of time, and from the time the signal SR1 ~~turns to the~~ is set to a low level, when the signal SR1 falls twice continuously from ~~the~~ a high level to ~~the~~ a low level at an interval T2, namely ~~of~~ less than an average of 1.5 second ~~average~~, ~~raises~~ sets the operation check function control signal SS to ~~the~~ a high level.

[0086] This operation is described ~~by~~ with reference to FIGs. 6A and 6B.

[0087] At the initial state, the output signal Q of the SR latch 406~~has the~~is at high level, both the output signals Q0 and Q1 of the counter 402 ~~have the~~ are at a low level, the signal SS ~~has the~~ is at a low level, the output signal of the ~~double~~dual-input XNOR gate 411 ~~has the~~ is at a high level, both the output signals Q0 and Q1 of the counter 401 ~~have the~~ are at a low level, and the output signal Q of ~~the~~ D ~~flip-flap~~flip-flop 405 ~~has the~~ is at a low level.

[0088] ~~Here, when~~ When the crown is pulled out to the second click, the signal SR1 ~~becomes the~~ is set to a high level. As a result, the output signal of ~~the~~ AND gate 412 ~~becomes the~~ is set to a high level, and the reset of the counter 403 and the D ~~flip-flap~~flip-flop 404 are cancelled.

[0089] After this cancellation, when the first clock pulse F1 is generated, ~~by this clock pulse F1 counting of the~~ counter 403~~is carried out~~ counts this clock pulse F1~~,~~ ~~and the~~ causing its output signal XQ ~~of the counter 403~~ to fall~~s~~ (~~the~~ arrow a1).

[0090] ~~Then, w~~When the second clock pulse F1 is generated, ~~counting of the~~ counter 403 ~~is carried out further~~ counts this pulse~~,~~ and ~~the~~ its output signal XQ ~~of the counter 403~~ rises (the arrow a1). As a result, ~~the~~ a high level signal is input to ~~the~~ the clock in put of D flip-flop 404, and ~~the~~ output ~~signal~~ Q of the D flip-flop 404 rises (~~the~~ arrow a3). Then due to ~~by~~ this rise ~~of~~ in the output ~~signal~~ Q of ~~the~~ D flip-flop 404, ~~the~~ SR latch 406 is reset, and the output ~~signal~~ Q of ~~the~~ SR latch 406 ~~becomes the~~ is reset to a low level (~~the~~ arrow a4). ~~And b~~Because the output of SR latch 406 ~~becomes the~~ is reset to a low level, the reset state of ~~the~~ counter 402 is cancelled, and ~~the state of the~~ counter 402 enters a state where it can actively count ~~becomes practicable to counting~~.

[0091] Next, when the crown is pushed back from the second click to the first click or to the normal position, the signal SR1 falls to ~~the~~ a low level. As a result, ~~the~~ counter 403 and ~~the~~ D ~~flip-flap~~flip-flop 404 are reset, and ~~the~~ output ~~signal~~ Q of the D ~~flip-flap~~flip-flop 404 ~~becomes the~~ is set to a low level.

[0092] On the other hand, when ~~the~~ pulse signal SR2 is generated by the fall of ~~the~~ signal SR1, ~~the~~ pulse signal SR2 starts ~~the~~ counter 402~~ to conduct the counting up~~, and the output ~~signal~~ Q0 of ~~the~~ counter 402 rises to ~~the~~ a high level (~~the~~ arrow a6). As a result, the output signal of ~~the~~ XNOR gate 411 ~~becomes the~~ is set to a low level (~~the~~ arrow a7). Thus the reset state of ~~the~~ counter 401 is cancelled, and ~~the state of the~~ counter 401~~ becomes practicable to counting~~ is set to an active counting state, i.e. a state where it can actively count.

[0093] As described above, after the crown is pulled out to the second click, when two clock pulses F1 are generated, ~~the state of the~~ counter 402 is set to its active

counting state~~ becomes practicable to counting~~. Then when the crown is pushed back to the first click or to the normal position, the ~~state of the~~ counter 401 ~~becomes practicable to~~ is set to its active counting state.

[0094] In the above description, in the period from the rise to the fall of the signal SR1, two clock pulses F1 are generated. However, a case where three or more clock pulses F1 are generated ~~falls into the same~~ has a similar result.

[0095] Afterward, if the crown is not ~~handled~~ adjusted, ~~the~~ signal SR1 does not change, and ~~the~~ clock pulse F1 is generated, then ~~counting up is carried out at the~~ counter 401 will continue to count~~,~~ and ~~the~~ its output ~~signal~~ Q0 ~~of the counter 401 becomes the~~ will be set to a high level (the arrow a8). Then ~~when the~~ if another clock pulse F1 is generated ~~further~~, ~~counting up is carried out at the~~ it will be counted by counter 401~~, and the~~ resulting in output ~~signal~~ Q0 of ~~the~~ counter 401 ~~becomes the~~ being set to a low level, and ~~the~~ output ~~signal~~ Q1 of ~~the~~ counter 401 ~~becomes the~~ being set to a high level (~~the~~ arrow a9).

[0096] Then because the output signal Q1 of the counter 401 ~~becomes the~~ is set to a high level, the output ~~signal~~ Q of ~~the~~ SR latch 406 ~~become the~~ is set to a high level (~~the~~ arrow a10). As a result, ~~the~~ counter 402 is reset, ~~the~~ output ~~signal~~ Q0 of ~~the~~ counter 402 ~~becomes the~~ is set to a low level (~~the~~ arrow a11), and the output ~~signal~~ of ~~the~~ XNOR gate 411 ~~becomes the~~ is set to a high level (~~the~~ arrow a12).

[0097] Then because the output signal of ~~the~~ XNOR gate 411 ~~becomes the~~ is set to a high level, ~~the~~ counter 401 is reset (~~the~~ arrow a13)~~,~~ and ~~afterward the counter~~ will not count even if ~~the~~ clock pulse F1 is ~~given~~ generated.

[0098] As described, even when ~~the~~ counters 401 and 402 ~~become practicable to counting~~ are set to their active counting state by pulling the crown to the second click and pushing it back to the original position, if the crown is not ~~handled~~ adjusted, the operation check function control circuit 310 returns to the state before ~~handling~~ adjusting the crown, and ~~the~~ signal SS does not change.

[0099] ~~Compared to this~~In comparison, when ~~the~~ counters 401 and 402 ~~become practicable to counting~~ are set to their active counting state by pulling the crown to the second click, if a prescribed crown ~~handling is done~~adjusting is carried out, ~~the~~ signal SS is raised by the operation check function control circuit 310.

[0100] ~~From here,~~ FIG. 6B ~~is~~ will now be described. ~~The o~~Operations ~~with the~~ relating to arrows a1 to a7 are the same as ~~in~~ those described with reference to FIG. 6A.

[0101] As described in FIG. 6A, after the crown is pulled out to the second click, when two clock pulses F1 are generated, ~~the state of the~~ counter 402 is placed in its

active counting state~~becomes practicable to counting~~. Then when the crown is pushed back to the first click or to the normal position, ~~the state of the~~ counter 401 ~~becomes practicable to~~ is placed in its active counting state (~~the~~ arrows a1 to a7).

[0102] Afterward, if the clock pulse F1 is generated, ~~counting up at the counter 401 is carried out by~~ this clock pulse F1 is counted by counter 401, and the ~~number~~count value ~~of count~~ of ~~the~~ counter 401 becomes "1" (~~the~~ arrow a11). ~~But~~ However, ~~before the next clock pulse F1 is generated,~~ if ~~the~~ pulse SR2 is generated by ~~the handling of~~ adjusting the crown before the next clock pulse F1 is generated, ~~the~~ counter 401 ~~is~~ will be reset~~,~~ and ~~the~~ its count value ~~number of count of the counter 401~~ will becomes "0" (~~the~~ arrow a12). ~~And counting up at the c~~Counter 402 ~~is carried out by the~~ counts pulse SR2, and the ~~number~~count value ~~of count~~ of ~~the~~ counter 402 will becomes "2" (~~the~~ arrow a13).

[0103] ~~Then w~~When ~~the~~ clock pulse F1 is again generated, it will be counted ~~counting up at the~~ by counter 401, whose ~~is carried out by this clock pulse F1, and the number~~count value ~~of count of the counter 401~~ will becomes "1" (~~the~~ arrow a14). But ~~before the next clock pulse F1 is generated,~~ if ~~the~~ pulse SR2 is generated by the ~~handling of~~ adjusting the crown before the next clock pulse F1 is generated, ~~the~~ counter 401 ~~is~~ will be reset~~, and the number of count of the counter 401~~ its count value will becomes "0" (~~the~~ arrow a15). Also, ~~And counting up at the~~ counter 402 ~~is carried out by the~~ will count pulse SR2, and ~~the~~ its ~~number~~count value ~~of count of the counter 402~~ will becomes "3" (~~the~~ arrow a13). As a result, ~~the~~ signal SS ~~becomes~~ will be set to a ~~the~~ high level (~~the~~ arrow a17). By this, the operation mode of the ~~electrical~~electric timepiece ~~becomes the~~ is set to mode 1, ~~. And~~ and the reset state ~~at the~~ of D ~~flip-flap~~flip-flop 405~~, the reset~~ is cancelled.

[0104] When the ~~number~~count value ~~of count~~ of ~~the~~ counter 402 becomes "3", the output ~~signal~~ of ~~the~~ XNOR gate 411 ~~becomes the~~ is set to a high level (~~the~~ arrow a18). As a result, ~~the~~ counter 401 is reset. Therefore, ~~afterward if the~~ further generations of clock pulse F1 ~~is generated, counting operation at the~~ will not be counted by counter 401 until it is set active again ~~will not be carried out~~.

[0105] As described above and shown in Fig. 6B, three conditions are required to set signal SS to a high level. Firstly, ~~if in~~ during ~~the~~ a period from the rise to the fall of ~~the~~ signal SR1, two or more clock pulses F1 are generated.~~,~~ ~~after~~ Secondly, another ~~the~~ rise and fall pulse of ~~the~~ signal SR1 is generated followed by another F1 pulse. ~~, and~~ Thirdly before the generation of ~~the~~ a subsequent clock pulse F1, ~~the~~ another rise and fall pulse of ~~the~~ signal SR1 (the pulse SR2) takes place, ~~and before the generation of the next clock pulse F1, the fall of the signal SR1 (the pulse SR2) takes place, the~~ by which signal SS is ~~switched~~ set to ~~the~~ a high level. Here,

because the ~~cycle~~ period of ~~the~~ clock ~~pulse~~ F1 is one second, the time period from the rise of ~~the~~ signal SR1 to the fall of ~~the~~ signal SR1, or the time period T1 in FIG. 7, will be fully ~~satisfied~~ complete within two seconds.

[0106] The time period from the first fall to the second fall of the signal SR1, or the time period from the third fall to the fourth fall of the signal SR1, or the time period T2 in FIG. 7, will be ~~satisfied~~ completed within 1.5 seconds.

[0107] Next, the state when the operation check function mode select result signal SV2 ~~has the~~ is at a low level, and the operation check function control signal SS ~~has the~~ is at a high level will be described.

[0108] In this case, when the signal SR1 rises, the mode 1 is cancelled. This operation is described in reference to in FIG. 6B.

[0109] First, when the signal SR1 rises, ~~the~~ a high level signal is input to ~~the~~ D flip-flop 405, and the output ~~signal~~ Q of ~~the~~ D flip-flop 405 becomes ~~the~~ is set to a high level (~~the~~ arrow a21). As a result, ~~the~~ SR latch 406 is set (~~the~~ arrow a22), output a high signal at its output and thereby ~~this the~~ placing counter 402 ~~is~~ in a reset state. As a result, ~~and~~ the ~~number~~count value of ~~count of the~~ counter 102 becomes "0" (~~the~~ arrow a23). Then because ~~the~~ counter 402 is in its reset state, ~~the~~ signal SS ~~becomes the~~ is set to a low level, and ~~the~~ mode 1 is cancelled (~~the~~ arrow a24).

[0110] ~~And because the~~ Since signal SS ~~becomes the~~ is at a low level, ~~the~~ D ~~flip-flap~~flip-flop 405 is reset (~~the~~ arrow a25). The subsequent operation ~~after this differs depending~~ depends on ~~what kind of~~ the wave form ~~is formed by the~~ of signal SR1, ~~but~~ and is described ~~already~~ above.

[0111] Next, reference to FIGS. 4 and 7, the state when the operation check function mode is ~~at the~~ to mode 2, and the operation check function mode select result signal SV2 ~~becomes the~~ is at a high level will be described.

[0112] In this case, even if the signals SR1 and SR2 changes, the operation check function control signal SS ~~does not turn to the~~ is not set to a low level.

[0113] Next, ~~referring~~ with reference to FIG. 5 ~~the~~ a detailed description will be given with respect to the second external input unit measure circuit 311, the operation check function mode select circuit 312, the stored electricity unit discharge control circuit 305, the stored electricity unit charging completion judge circuit 306, and the motor drive trouble judge circuit 304.

[0114] The second external input unit measure circuit 311 comprises an inverter 501, a ~~double~~dual-input AND gate 502, and a 2-bit counter 503. The inverter 501

receives the operation check function control signal SS. The AND gate 502 receives the second external input signal ST and the operation check function mode select result signal SV3. Here, the second external input signal ST is a signal ~~which becomes the~~ that is set to a high level when the switch (indicator switch) of the second external input unit G is pushed back. The output of inerter 501 is applied to the reset input of ~~As for~~ the 2-bit counter 503~~, in the reset terminal R enters an output signal of the inverter 501~~, and the output of AND gate 502 is applied to ~~in~~ the clock input of the 2-bit counter 503~~terminal enters an output signal of the AND 502~~. Therefore, ~~when the~~ both signals SS ~~has the high level and the signal~~ and SV3 ~~has the~~ are at a high level, the 2-bit counter 503 is placed in its active counting state and counts the number of pulses~~ (the number how many times the indicator switch is pushed back)input as the~~ of second external input signal ST (i.e. the number of many times the indicator switch is pushed back). ~~Here, the s~~Signal SV3 is ~~a signal~~ generated by decoding the output of ~~the~~ counter 503, and it is set ~~becomes the~~ to a low level when the ~~number~~count value ~~of count~~ of ~~the~~ counter 503 is 2. Therefore, ~~the~~ counter 503 counts ~~the value~~ from 0 to 2.

[0115] In an explanatory example of FIG. 7, after the operation check function control signal SS ~~becomes the~~ is set to a high level at ~~the~~ time t1, ~~the bits~~ bit signals SU1 ~~(Q0)~~ and SU2 at respective outputs ~~(~~ Q0 and Q1~~)~~ of ~~the~~ counter 503 ~~has been the~~ are set at low levels. At ~~the~~ time t2, as the signal ST, a pulse signal is input to the counter 503, ~~the~~ bit SU1 of the counter 503 ~~becomes the~~ is set to a high level and ~~the~~ bit SU2 of the counter 503 ~~becomes the~~ is set to a low level. At the time t3, as the signal ST, another pulse signal is input to the counter 503, the bit SU1 of the counter 503 becomes the low level and the bit SU2 of the counter 503 ~~becomes the~~ are set to a high level. When the bit SU1 ~~becomes the~~ is set to a low level and the bit SU2 ~~becomes the~~ is set to a high level, the signal SV3 ~~becomes~~ is set to a low level. In this case, for example, even if, as the signal ST, a pulse signal is input to the counter 503, the output value of the counter 503 does not change. The counter 503 is reset when the signal SS ~~becomes the~~ is set to a low level (at ~~the~~ time t5).

[0116] The operation check function mode select circuit 312 in FIG. 5 comprises an 3-input AND gate 504 (having ~~three input of~~ two ~~negative logic~~ active low inputs and one ~~positive logic~~ active high input), an 3-input NAND 506 (having ~~three input of~~ one ~~negative logic~~ active low inputs and two ~~positive logic~~ active high inputs). Bits SU1 and SU2 of counter 503 are applied to the ~~In~~ two ~~negative logic~~ active low inputs of ~~the~~ AND gate 504~~ enter bits SU1 and SU2 of the counter 503~~, and the operation check function control signal SS ~~in one positive logic~~ is applied to the active high input of ~~the~~ AND gate 504~~ enters the operation check function control signal SS~~. As shown in FIG. 7, when both the bits SU1 and SU2 of the counter 503

~~has the~~ are at a low level and the operation check function control signal SS ~~has the~~ is at a high level, the AND gate 504 outputs the operation check function mode select result signal SV1 ~~with the~~ at a high level indicating the operation check function is at ~~the~~ mode 1. In the same way, when the bit SU2 of the counter 503 ~~has the~~ is at a low level and both the bit SU1 and the operation check function control signal SS ~~has the~~ are at a high level, the AND gate 505 outputs the operation check function mode select result signal SV2 ~~with the~~ at a high level indicating the operation check function is at the mode 2. When the bit SU1 of the counter 503 ~~has the~~ is at a low level and both the bit SU2 and the operation check function control signal SS ~~has the~~ are at a high level, the NAND gate 506 outputs the operation check function mode select result signal SV3 ~~with the~~ at a high level indicating the operation check function is at the mode 3.

[0117] The stored electricity unit discharge control circuit 305 comprises an inverter 507, a D flip-flop 508, a ~~double~~dual-input AND gate 509, and a ~~triple~~3-input AND gate 510.

[0118] ~~In the inverter 507 enters a v~~Voltage detect result signal SN1 is input to inverter 507. ~~The s~~Signal SN1 ~~is one of~~ comes from one the bit lines of the voltage detect result signal SN. The signal SN1 ~~becomes the~~ is set to a high level, when ~~the detection is made~~ it is detected that the signal SC ~~of~~ indicating the stored voltage VKTN becomes lower than the discharge reference voltage DCHRGV (further from the ground VDD, that is, not reaching the predetermined discharge voltage). ~~Incidentally~~It is to be noted, instead of the above configuration, it is also possible to ~~make~~ set the signal SN1 ~~the~~ to a high level, when ~~the detection is made~~ it is detected that the stored voltage raising and lowering result signal SD which indicates the output voltage VSS of the raising and lowering circuit 49 becomes lower than the discharge reference voltage DCHRGV.

[0119] ~~As for~~ Regarding ~~the~~ D flip-flop 508, the operation check function mode select result signal SV1 is input to~~in~~ the reset terminal R ~~having the low active enters the operation check function mode select result signal SV1,~~ and the output signal of inverter 507 is input to ~~in~~ the clock terminal CLK ~~enters the output signal of the inverter 507~~, and the data input terminal D is fixed at ~~the~~ a high level.

[0120] ~~The~~ AND gate 509 ~~outputs a logical product~~ outputs the logic AND function of ~~the output signals of the~~ output ~~terminal~~ XQ of ~~the~~ D flip-flop 508 and the operation check function mode select result signal SV1 as the first stored electricity unit discharge control signals SO1.

[0121] ~~The~~ AND gate 510 ~~comprises a negative logic~~ has an active low input and two ~~positive logic~~ active high inputs. ~~Into the negative logic input enters t~~The first

stored electricity unit discharge control signals SO1 from ~~the~~ AND gate 509 is applied to the active low input of AND gate 510. ~~Into the positive logic inputs enters t~~The operation check function mode select result signal SV1 and the discharge reference voltage DCHRGV are applied to the active high inputs of AND gate 510. ~~The~~ AND gate 510 outputs ~~a~~ the logical AND function ~~product~~ of ~~the~~ its input signals as the second stored electricity unit discharge control signals SO2.

[0122] As shown in FIG. 7, the stored electricity unit discharge control circuit 305 ~~makes~~ sets the first stored electricity unit discharge control signals SO1 ~~the~~ to a high level when operation check function mode shifts to the mode 1 ~~under the condition~~ when the battery unit (battery 48) is being charged.

[0123] In a period P1 when the first stored electricity unit discharge control signals SO1 ~~has the~~ are at a high level, the timepiece control circuit 303 in FIG. 3 outputs as the motor driving signal SF a drive clock signal which short-circuits the motor dive circuit E or fast-forwards the motor unit D. Accordingly, ~~in~~ during ~~the~~ period P1 in FIG. 7, the ~~electrical~~electric charge in ~~the~~ battery unit 48 is released ~~to be~~ as a drive current on a scale much ~~larger~~ higher than that ~~at~~ of the normal drive state ~~in~~ of the motor unit D.

[0124] As discharging continues, when the stored electricity voltage VTKN or the stored electricity voltage raising and lowering result voltage VSS becomes higher than the discharge reference voltage DCHRGV (that is, nearer to the ground VDD, meaning the discharging ~~advanced~~ operation is progressing), the signal SN1 ~~becomes the~~ is set to a low level synchronous ~~to~~ with the voltage detect control signal SX, which is repeatedly ~~becomes the~~ set to a low level in a predetermined cycle. When the signal SN1 ~~becomes the~~ set to a low level, the stored electricity unit discharge control circuit 305 ~~makes~~ sets the first stored electricity unit discharge control signals SO1 ~~the~~ to a low level. ~~By this~~Thus, the period P1 shifts to a period P2.

[0125] When the first stored electricity unit discharge control signals SO1 ~~becomes the~~ are set to a low level, the timepiece control circuit 303 in FIG. 3 outputs for example a signal to stop the motor drive unit E. Accordingly, ~~in the~~ during period P2, discharging of ~~the~~ battery unit 48 is stopped, and the stored electricity voltage VTKN or the stored electricity voltage raising and lowering result voltage VSS ~~becomes to the~~ is gradually brought to a low voltage ~~gradually~~ by the voltage recovery effect. Then when the voltage VTKN or VSS becomes lower than the discharge reference voltage DCHRGV, the signal SN1 ~~becomes the~~ is set to a high level synchronous ~~to~~ with the voltage detect control signal SX, and the second stored

electricity unit discharge control signals SO2 ~~becomes the~~ is set to a low level. By this, the period P2 shifts to a period P3.

[0126] ~~Incidentally~~It is to be noted that, although not shown in FIG. 3, the operation check function control signal SS and the operation check function mode select result signal SV and the like are supplied to the timepiece control circuit 303. The timepiece control circuit 303 is capable of distinguishing the shifting state between each mode by these control signals.

[0127] When the second stored electricity unit discharge control signals SO2 ~~becomes the~~ are set to a high level, the timepiece control circuit 303 in FIG. 3 outputs, as the motor driving signal SF, a drive clock signal to fast-forward the motor unit D. Here, ~~as~~ fast-forwarding modes~~,~~ include ~~there are a~~ 32 hertz fast-forwarding, an intermittent drive of 32 hertz drive and stop, ~~and~~ 8 hertz fast-forwarding, and the like. ~~In a period~~ During P3, the ~~electrical~~electric charge of the battery unit 48 is re-released to be a drive current on a scale of smaller than that of the period P1 and larger than that at the normal drive state.

[0128] Then, when the voltage VTKN or VSS again becomes higher than the discharge reference voltage DCHRGV ~~again~~, the signal SN1 ~~becomes the~~ is set to a low level at ~~the~~ a timing synchronous ~~to~~ with the voltage detect control signal SX, and the second stored electricity unit discharge control signals SO2 ~~becomes the~~ are set to a low level. ~~By this~~Thus, ~~the~~ period P3 shifts to ~~a~~ period P4.

[0129] When the second stored electricity unit discharge control signals SO2 ~~has the~~ are at a low level, the timepiece control circuit 303 stops the motor drive circuit E. Therefore, ~~in the~~ during period P4, discharging of the battery unit 48 is stopped, and the stored ~~electricity~~ voltage VTKN of the battery unit 48 or the stored ~~electricity voltage~~ raising and lowering result voltage VSS is again gradually brought ~~becomes~~ to the low voltage ~~gradually~~ by the voltage recovery effect ~~again~~. Until the stored voltage becomes stable or the shift to ~~the~~ mode 2 is carried out by the external input, the ~~states~~ operations performed during ~~of the~~ periods P3 and P4 ~~is~~ are repeated and the discharging is carried out. However, in the example of ~~But~~ FIG. 7, ~~shows an example that~~ after one repeat operation ~~the~~ a shift to the mode 2 is conducted.

[0130] Next, the stored electricity unit charging completion judge circuit 306 shown in FIG.5 will be described. The circuit 306 is composed of an AND gate 511, and outputs as the stored electricity unit charge completion control signal SP a logical ~~product~~ AND function of the voltage detect result signal SN2 and the operation check function mode select result signal SV2. Here, the signal SN2 is a signal output from the voltage detecting circuit 302 ~~and becomes the~~ and is set to a

high level when the stored electricity voltage VTKN or the stored voltage raising and lowering result signal SD (VSS) becomes lower than the charge reference voltage CHRGV (that is, further from the ground VDD, or reaching the predetermined discharge voltage). The signal SV2 is a signal output from the operation check function mode select circuit 312 and ~~becomes the~~ is set to a high level when the mode is 2. Accordingly, the signal SP becomes ~~the~~ is set to a high level when the operation check function is at mode 2 and the stored electricity unit 48 is charged until ~~the~~ it reaches charge reference voltage CHRGV.

[0131] In ~~the~~ mode 2 in the timing chart of FIG. 7, a vibration is given to the timepiece from outside, and electricity is generated in the generator system A. Therefore ~~the~~ charging ~~to~~ of the battery unit 48 is conducted, and the stored ~~electricity~~ voltage VTKN ~~is going~~ goes down (period P5). During this time, the timepiece control circuit 303 supplies for example a prefixed pulse signal to the motor ~~dive~~ drive circuit E, and ~~controls~~ causes the motor unit D to ~~the~~ perform normal hand movement (one-second interval movement).

[0132] Charging continues, and when the stored ~~electricity~~ voltage VTKN or the stored ~~voltage~~ raising and lowering result voltage signal SD (VSS) becomes lower than the charge reference voltage CHRGV, the signal SN2 ~~becomes the~~ is set to a high level synchronous ~~to~~ with the voltage detect control signal SX. ~~And~~ Additionally, the stored electricity unit charge completion control signal SP ~~becomes the~~ is set to a high level. ~~By this~~Thus, ~~the~~ period P5 shifts to ~~a~~ period P6.

[0133] When the stored electricity unit charge completion control signal SP ~~becomes the~~ is set to a high level and the ~~stage~~ operation enters into ~~the~~ period P6, the timepiece control circuit 303 supplies, for example, the motor driving signal SG to the motor dive circuit E, and controls the hand movement state of the motor unit D to for example two-second interval movement which is different from the normal hand movement (in this case, one-second interval movement). By this change of the hand movement ~~state~~operation, ~~the~~ notification of ~~the~~ completion of ~~the~~ charging is ~~made~~provided. ~~Incidentally~~It is to be noted that, in ~~the~~ period P6, if the charging voltage increases (that is, discharging is conducted), charging is conducted in the same way as ~~the~~ in period P5. Accordingly, in ~~practical~~ practice, ~~the~~ periods P5 and P6 ~~is~~ are repeated, and the charging voltage becomes stable.

[0134] Next, the motor drive trouble judge circuit 304 shown in FIG.5 will be described. ~~The c~~Circuit 304 comprises ~~double~~dual-input AND gates 512 and 513~~,~~ (both having ~~a positive logic~~ one active-high input and ~~a negative logic~~ active-low input), a triple-input OR gate 514, a ~~double~~dual-input OR gate 515, and a 3-bit counter 516.

[0135] ~~The~~ AND gate 512 receives the non-rotation detect measure signal SY ~~as a positive logic~~ at its active-high input terminal, and the high-frequency magnetic field detect result signal SK or the alternating current magnetic field detect result signal SL ~~as a negative logic~~ at its active-low input terminal. Here, the signal SY is a signal generated when ~~the~~ non-rotation in the motor unit D is detected. The signals SK and SL ~~becomes the~~ are set at high levels when a magnetic field is detected.

[0136] ~~The~~ AND gate 512 receives the rotation detect result signal SM as at its active-low ~~positive logic~~ input terminal, and receives ~~an~~ output ~~bit~~ Q2 of ~~the~~ counter 516 ~~as a negative logic~~ at its active-low input terminal. Here, the signal SM ~~becomes the~~ is set to a high level when ~~the~~ non-rotation in ~~the~~ motor unit D is detected. The output ~~bit~~ Q2 of ~~the~~ counter 516 ~~becomes the~~ is set to a high level when the counter number of ~~the~~ counter 516 becomes 4 or more.

[0137] ~~The~~ OR gate 514 receives the output ~~signal of the~~ AND gate 512, the operation check function mode select result signal SV3, and ~~the~~ output ~~bit~~ Q2 of ~~the~~ counter 512.

[0138] ~~The~~ OR gate 515 receives the output ~~signal of the~~ AND gate 513 and the operation check function mode select result signal SV3.

[0139] The operation of the motor drive trouble judge circuit 304 configured as explained above will be described by reference to FIG. 7 as follows.

[0140] In FIG. 7, ~~at the~~in mode 2, when the indicator switch is pushed on, operation shifts to ~~the~~ mode 3 ~~is carried out~~ (~~the~~ period P6 to period P7). In this mode ~~4~~ 3, the operation check function mode select result signal SV3 ~~becomes the~~ is set to an active level (low level), and the reset state of the counter 516 of the motor drive trouble judge circuit 304 is cancelled.

[0141] ~~At the~~ In mode 3, ~~the~~ quality verification of the operation state under high and low temperatures ~~condition~~ is carried out. ~~The q~~Quality verification is carried out as follows.

[0142] First, the timepiece control circuit 303 in FIG. 3 supplies the motor drive signal SE to the motor drive circuit E, and conducts a normal control of the motor unit D (one-second interval movement, rotation detect, drive by auxiliary pulse under a certain condition, and the like).

[0143] Here, this supply of the motor drive signal SE ~~rotates~~ causes the motor to rotate. And when the rotation is detected, the rotation detect result signal SM is output from the rotation detect circuit 309, and thus the counter 516 is reset.

[0144] On the other hand, if the motor does not rotate ~~with the supply of the~~ when signal SE is supplied, pulse signals including the auxiliary pulse having ~~bigger effective electric~~ more power than the normal driving pulse are automatically supplied to the motor drive unit D from the timepiece control circuit 303, and at the same time the timepiece control circuit 303 outputs the non-rotation detect measure signal SY.

[0145] ~~The c~~Counter 516 counts the number of ~~generation~~ times~~of the~~ signal SY is generated.

[0146] When the non-rotation detect measure signal SY ~~enters into the~~ is applied to counter 516 four times successively while ~~under a condition of no detection of~~ no rotation is detected, ~~the~~ output ~~bit~~ Q2 of ~~the~~ counter 516 ~~becomes the~~ is set to a high level, and the motor drive trouble judge signal SQ indicating that the motor has a problem is output.

[0147] The timepiece control circuit 303, when the motor drive trouble judge signal SQ ~~becomes the~~ is at a high level, supplies to the motor drive circuit E, for example, the motor drive signal SH for ~~controlling~~ causing the motor unit D to implement two-second-interval hand movement which is different from the normal hand movement of one-second-interval hand movement.

[0148] On the other hand, when the motor drive trouble judge signal SQ ~~becomes the~~ is set to a high level, the counter 516 no longer receives a reset signal and a clock signal. Therefore, the counter 516 stops counting. The signal SQ maintains ~~the~~ a high level until ~~the~~ mode 3 is cancelled and the operation check function mode select result signal SV3 ~~becomes the~~ is set to a high level.

[0149] ~~Namely~~Specifically, even after the quality verification operation ~~under~~ at high and low temperatures ends, and the temperature becomes normal ~~temperature~~, as long as ~~the~~ mode 3 is maintained, drive signals causing a ~~having different~~ hand movement ~~state~~ different from the normal hand movement ~~is~~ supplied to the motor unit D.

[0150] Accordingly, after the quality verification operation, notification of the motor drive trouble that occurred during the quality verification operation continues to be made.

[0151] Next, the motor driving signal SF for discharging the battery unit will be described by reference to FIG. 8.

[0152] FIG. 8 is a block diagram showing the timepiece control circuit 303 shown in FIG. 1, the motor drive circuit E and the motor unit D. The motor drive circuit E comprises switches 701 to 705 and 707, and rotation detect use elements 706 and

708. In the example shown in FIG. 8, switches 701, 703, 705, and 707 are P-channel MOS (metal oxide semiconductor) transistors, and switches 702 and 704 are N-channel MOS transistors.

[0153] Four switches 701 to 704 form a bridge circuit which drives the stator winding of the motor unit D by use of a potential difference between VDD and VSS as source voltage.

[0154] Rotation detect use elements 706 and 708 are elements to place restrictions on current flowing through the motor unit D, and are comprised of resistors and the like.

[0155] Switch 705 and rotation detect use element 706 are connected in series between one terminal of the motor coil of the motor unit D and the power source line VDD. Switch 707 and rotation detect use element 708 are connected in series between the other terminal of the motor coil of the motor unit D and the power source line VDD

[0156] ~~By the above configuration, in order t~~To ~~make~~ cause short-circuit current to flow in the motor drive circuit E (for the purpose of discharging the battery unit 48) using the above configuration, ~~by turning the~~ switches 701 and 704 are turned on~~, it is possible~~ to ~~make the~~ cause short-circuit current O1 to flow in accord with the load of the motor unit D. By turning on ~~the~~ switches ~~701~~ 703 and 702~~704 on~~, it is also possible to ~~make~~ cause ~~the~~ short-circuit current O2 to flow in accord with the load of the motor unit D. And by making one of short-circuit currents O1 or O2 flow constantly, or by making short-circuit currents O1 and O2 flow by turns at a predetermined fast-forwarding cycle, it is possible to control the short-circuit current.

[0157] When required to generate a comparatively small discharge current, it is possible to ~~make~~ establish discharge current flow ~~to the~~ through motor unit D via ~~the~~ rotation detect use elements 706 or 708.

[0158] Next, one example of the operation check method of the electronic timepiece explained above will be described by reference to FIG. 9A, 9B, 9C, and 10. FIGs. 9A, 9B, and 9C ~~cooperate to~~ collectively form a flowchart showing flow of operation check process of the electronic timepiece. The flowchart shows the check procedure of processes B101, B104, and B105, which comprise the operation check process B100 shown in the FIG. 2. FIG. 10 shows a specification of the operation check process in FIGs. 9A, 9B, and 9C.

[0159] With ~~R~~reference to FIGs. 9A, 9B, and 9C, ~~when~~ the timepiece is ~~under~~ in the normal operation drive state ~~(~~ in step 801~~)~~, and is shifted to mode 1 by specific

operation of the crown in step 802 (i.e. ~~operation for commanding to~~ a shift to the mode 1 is commanded, as shown in FIG. 10, ~~that is to~~ by pulling out the crown by two clicks and pushing it back for a predetermined time period)~~, is done (step 802)~~. As a result, the mode 1 (battery discharge mode) starts. ~~Here, discharging by~~ In mode 1, the drive is discharged by using, for example, a fast-forwarding pulse ~~with~~ of 32 hertz (step 803). ~~By~~ Due to this discharging, when the absolute value of the stored voltage VTKN ~~declines~~ falls below a ~~prefixed~~ predetermined voltage (~~in FIG. 10,~~ i.e. 1.25V in Fig. 10), the drive in the motor unit D is stopped~~s~~ (step 804). In ~~practical~~practice, the ~~fast-forwarding~~ drive discharging operation in step 803 has two steps: ~~of~~ the first being ~~the~~ a continuous fast-forwarding discharge~~ing~~; and the second being a discharge~~ing~~ by repeated~~ing~~ stopping and starting of the fast-forwarding discharge ~~and stoppage by turn at a~~ at two second~~-cycle~~ intervals. ~~And when~~ If the voltage of the battery 48 ~~returns~~ drifts upward, ~~the~~ steps 803 and 804 are ~~carried out again and then~~ repeated~~ly~~ until the voltage ~~will not return~~ no longer drifts. It will take for example several tens of hours discharging until the discharged state becomes stable at ~~the state of the~~ step 804. ~~Incidentally~~It is to be noted that~~,~~ the time period necessary to discharge differs depending on the type of battery, as shown in FIG. 10, but several tens of hours is adequate. Therefore after discharging for a predetermined time period of several tens of hours, by checking the hand movement state, it is possible to ~~judge~~ determine whether or not the discharging operation is completed. In this example, as shown in FIG. 10, when repeated~~ly~~ fast-forwarding and ~~stoppage~~ stopping is occurring, it is possible to ~~judge~~ determine that the discharging operation is completed, and when continuously fast-forwarding is occurring, it is possible to ~~judge~~ determine that the discharging operation is not completed.

[0160] After completion of the discharge, when the operator handles the indicator switch once (step 805), the mode shifts to the mode 2 (charging mode). In the mode 2, the motor unit D is driven (step 806) ~~in~~ using the normal hand movement method (one-second interval movement). During this period, by ~~giving~~ applying vibration, electricity is generated in the generator system A, and the battery 48 is charged (step 807). In ~~here~~ this step, charging for from several tens of minutes to several hours is carried out, and when the absolute value of the stored voltage VTKN becomes equal to or larger than ~~the~~ a predetermined voltage (in FIG. 10, 1.33 V), the normal hand movement state shifts to the two-second interval movement state (step 808). Therefore, after the predetermined time period, if the normal hand movement state is maintained, it is possible to ~~judge~~ determine that the charging function has a problem (step 809). In ~~here~~ this step, before the operation check of the mode 3, time adjusting is carried out (step 810). Time adjusting is ~~done~~

<u>accomplished</u> by, for example, pulling out the crown by two clicks and turning the crown. In the present embodiment, when the mode is at the mode 1 or 3, if the crown is operated, the operation check function is released. But, when the mode is at the mode 2, if the crown is operated ~~for~~ <u>to</u> adjust~~ing~~ time, the mode does not shift to <u>an</u>other mode.

[0161] Next, when the operator handles the indicator switch once (step 811), the mode shifts to the mode 3 (operation mode). In the mode 3, the motor unit D is driven (step 812) ~~in~~ <u>using</u> the normal hand movement. Then in the electronic timepiece, self-verification of the drive malfunction during operation is carried out by use of the auxiliary pulse (step 813). In ~~here~~ <u>this step</u>, when the successive pulse drive <u>does not require the use of</u> ~~by using~~ more than a predetermined <u>number of</u> auxiliary pulses ~~is not carried out~~ during operation, the electronic timepiece ~~judges~~ <u>determines</u> itself ~~as~~ <u>to be</u> normal and leaves the hand movement state in the one-second<u>-</u>interval movement (step 814). ~~By this~~<u>Thus</u>, the operator can ~~judge~~ <u>determine</u> that the electronic timepiece is in good quality. On the other hand, when the successive pulse drive <u>requires the use of</u> ~~by using~~ more than a predetermined <u>number of</u> auxiliary pulses ~~is carried out~~ during operation, the electronic timepiece ~~judges~~ <u>determines</u> itself ~~as~~ <u>to be</u> bad and ~~makes~~ <u>places</u> the hand movement state in the two-second<u>-</u>interval movement (step 815). ~~By this~~<u>Thus</u>, the operator can ~~judge~~ <u>determine</u> that the electronic timepiece is ~~in~~ bad ~~quality~~.

[0162] Next, when the operator performs a two-click crown pull-out (step 816), ~~the~~ mode 3 is cancelled, and ~~the~~ normal operation state is ~~recovered~~ <u>restarted</u> (step 817).

[0163] ~~Incidentally~~<u>It is to be noted that</u>~~,~~ ~~at the~~ <u>in</u> step 814, when ~~the~~ indicator handling is ~~carried out~~ <u>executed</u> twice (step 818), the movement ~~becomes~~ <u>is placed in</u> ~~the~~ one-second<u>-</u>interval movement <u>operation</u> (step 819). In this case, even if the charging is carried out next (step 820), the one-second hand movement continues (step 821) irrespective of the charging state. And ~~at the~~ <u>in</u> step 804, when ~~the~~ indicator handling is carried out three ~~times~~ or more <u>times</u> (step 822), the indicator for indicating the charging state is put into operation (step 823). ~~And a~~<u>A</u>lso, ~~at the~~ <u>in</u> step 810, it is conceivable that indicator handling is carried out twice or more <u>times</u> (step 824), or the operation state becomes that of ~~the~~ step 821 or 823. In these cases, when the crown is <u>next</u> handled ~~once next time~~ (step 825), the operation returns to the normal drive state of ~~the~~ step 801. By these check procedure<u>s</u>, even if the operator makes a mistake in inputting <u>an</u> operation with the indicator, it is impossible to ~~happen mis-judgement of the~~<u>identify a</u> poor quality product as <u>a</u> good quality one. For example, ~~at the~~ <u>in</u> step 804, ~~the~~ normall<u>y</u> ~~check~~

~~flow is first an~~ the indicator is handed~~ling~~ once ~~then shifting~~ to shift to ~~the~~ mode 2. However, it can happen that the operator ~~performs~~ handles the indicator ~~handling~~ twice by mistake. In this case, one-second interval movement takes place.~~,~~ ~~And~~ and the operator cannot tell whether ~~that~~ the movement is ~~of the~~ that of step 806 or step 819. ~~But~~ However, since the operator thinks that the indicator handling ~~is~~ was performed once, the operator thinks the mode is ~~at the~~ mode 2 and conducts charging. In this case, charging ~~at the~~ in step 820 ~~follows~~ is executed followed by ~~and then~~ one-second interval movement ~~at the~~ in step 821~~follows~~. ~~And~~ Since the operator mistakes ~~thinks the~~ step 809 for step 821~~as the step 809~~, and the operator determines ~~judges~~ that the electronic timepiece ~~to be in poor condition~~ is bad (in reality, since at the mode 1 the indicator is handled twice, the mode ~~is~~ was shifted to ~~the~~ mode 3, and not to mode 2). As ~~described~~ explained here, there are ~~cases~~ circumstances when ~~that~~ the check flow shifts to ~~the~~ step 825 due to ~~mis-judgement of the~~ a good quality product being misjudged as a poor quality one. But it is impossible to ~~mis-judge~~ misjudge ~~the~~ a poor quality product as a good quality one. ~~And~~ Furthermore, ~~the~~ a ~~mis-judged~~ good timepiece ~~as~~ that is misjudged as bad ~~poor quality is~~ will undoubtedly re-judged as good when the check routine is ~~redone~~ repeated starting from ~~the~~ step 825. ~~And~~ Additionally at ~~the~~ step 804, ~~when~~ if the indicator ~~handling~~ is handled ~~is performed~~ three times or more, ~~that is~~ as in the above case when the operator ~~performs~~ handled the indicator ~~handling three~~ two times ~~or more~~ by mistake, the third ~~indicator~~ handling of the indicator ~~is~~ signals, for example, an operation for starting the displaying of the charging amount indicator. Since ~~In~~ in this check operation flow~~, since~~ there is no process step ~~to~~ for starting the displaying of the charging amount indicator, the operator can tell immediately that the mode is not at ~~the~~ mode 2 due to the difference of the display. Therefore, the operator ~~thinks~~ recognizes that the indicator was mishandled~~ing is wrongly done~~, and proceeds to ~~the~~ step 825~~, then reconducts~~ and re-executes the check~~ing~~ operation flow. ~~On the other hand~~Furthermore, if the process flow is at the step 810~~,~~ and ~~if~~ the indicator ~~handling is performed~~ is handled ~~twice~~ two times or more, the second handling of the indicator ~~handling is~~ would typically signal an operation for starting the displaying of the charging amount indicator. However~~In~~ in this check flow, ~~since~~ there is no process to start the displaying of the charging amount indicator~~,~~ and the operator can therefore ~~tell~~ immediately recognize that the mode is not at the mode 3 due to the difference of the display. Therefore, the operator ~~thinks~~ recognizes that the indicator was mishandled~~ing is wrongly done~~, and proceeds to ~~the~~ step 825~~,~~ ~~then~~ and ~~re-conducts~~re-executes the check~~ing~~ flow.

[0164] As described above, ~~with~~ in the present embodiment, ~~at the~~ in mode 1, by ~~performing~~ applying an external input operation to the electronic timepiece,

discharging ~~is carried out~~ implemented by fast-forwarding drive in the motor unit D, or by short-circuiting of the motor drive circuit E, or the like. Accordingly, no special provision for discharging the battery is necessary. ~~And~~ Additionally, when the operational mode ~~becomes the~~ shifts to mode 1, the shift takes place from the normal hand movement state to the different state of fast-forwarding hand movement or hand movement stoppage. By ~~looking~~ observing the difference ~~of the~~ in hand movement, the mode shift is easily verified.

[0165] In the above embodiment, the external input operation is performed by use of the crown and the indicator switch. But the present invention is not limited to this. It is possible to use other mechanical input methods. ~~And it~~ It is also possible to ~~furnish~~ provide an infrared remote control receiver unit in the electronic timepiece, and use infrared signaling as the input method. Electricity, a radio wave, light, sound, an electromagnetic wave, heat, and the like are also ~~applicable~~ suitable as input methods.

[0166] In the above embodiment, discharging ~~at the~~ in mode 1 is continued until the battery voltage reaches the prescribed voltage. ~~And w~~When the battery voltage reaches the prescribed voltage, the discharging and the hand movement stop. Accordingly, by the hand movement (fast-forwarding or stoppage), ~~judging~~ it is possible to determine whether discharging ~~continues~~ is ongoing or discharging is completed. ~~And~~ Also, ~~by the battery voltage recovery effect~~ when the battery voltage drifts ~~exceeds~~ beyond the predetermined voltage~~,~~, due to the battery voltage recovery effect, discharging is resumed and is repeatedly ~~carried out~~ executed until the voltage ~~becomes~~ is returned to the predetermined voltage. ~~Accordingly, the~~ The battery voltage after discharging ~~becomes~~ is thereby made stable.

[0167] Also, in the above embodiment, two setting values of the discharging current amount are provided, heaving load discharging in ~~. At the~~ first stage ~~is heavy load discharging, at the second stage is~~ and light load discharging in the second stage. Therefore it is possible to control the battery voltage to the predetermined voltage in ~~less~~ a shorter time period. More than two setting values of the discharging current amount can be provided.

[0168] ~~And~~Furthermore, ~~at the~~ in mode 2, it is possible to shifting to the charging mode by operation of an external input on the electronic timepiece ~~is possible~~, and after ~~the~~ mode shifting, the operation is ~~done~~ executed in the normal hand operation state. ~~When~~ During a charging operation, when the voltage reaches the predetermined (i.e. completion) voltage level, ~~by changing the hand movement state the~~ a notification ~~is made~~ that ~~the~~ charging ~~is done~~ to the predetermined voltage level or ~~more~~ higher, has been achieved is made by changing the hand movement

state. The changing of the hand movement at this time is not limited to the above form, and can be arranged in any other form as long as it is possible to tell the difference of before and after charging completion.

[0169] ~~At the~~In mode 2, during the charging of the battery, ~~there is a false~~ the observed voltage ~~increase~~ rise can be false (i.e. transient). ~~Therefore~~That is, ~~even though~~ when the observed voltage ~~once~~ first reaches the completion voltage level, the battery voltage can ~~decline~~ gradually fall to ~~the~~ a real charged voltage ~~gradually~~ after completion of the charging (i.e. the charging operation is stopped). But~~,~~ in the present embodiment, in ~~the case~~ a situation where the charging voltage ~~once~~ reaches the ~~charging~~ completion voltage level ~~if~~ and the charging voltage then falls below the ~~charging~~ completion voltage level, ~~again~~ the hand movement again returns to the normal hand movement. Accordingly, after completion of the charging, by leaving the timepiece until the false battery voltage becomes the real voltage and then confirming the hand movement, it is possible to prevent a ~~mis-judgement~~ misinterpretations due to a false voltage ~~increase~~ high.

[0170] In the above embodiment, if ~~detection is made~~ it is successively detected that the motor does not rotate when ~~the~~ a normal motor drive pulse is supplied, a drive pulse having ~~bigger~~ greater effective electric power than the normal driving pulse is ~~supplied~~ applied. ~~And at the~~ In mode 3, if the drive pulse is successively output ~~successively~~ a predetermined number of times (or more), the ~~judgement~~ it is ~~made~~ determined that ~~the~~ a problem where the motor ~~trouble of~~ is not driven by application of ~~the~~ a normal drive pulse has occurred. Thus the hand movement is changed, and ~~the~~ notification of the motor ~~trouble~~ problem is made.

[0171] ~~At the~~ In mode 3, by operation of external input on the electronic timepiece, the mode is shifted to a poor quality detection mode, and the electronic timepiece is operated in a predetermined hand movement. Therefore, by changing the hand movement state of before and after this shift, it is made possible to easily confirm the mode shift.

[0172] ~~And~~Further, once the trouble is detected, the hand movement at the trouble detection is continued, therefore it is possible to easily confirm the result of trouble detection.

[0173] ~~And~~ Also, ~~at the~~ in mode 3, because it is possible to perceive the motor drive trouble by the hand movement, it is made possible to identify the trouble.

[0174] Also, it becomes possible to detect that the motor quality is somewhat lower than the satisfying quality but is not bad enough to cause stoppage (time keeping continuation trouble) or delay, both being difficult to detect hitherto. Therefore,

quality improvement is expected. Namely, if the motor quality is a bit poor and the detection of the non-rotation is frequently made, the motor will be driven by the auxiliary pulse having bigger effective electric power than the normal driving pulse. Therefore, time delay does not ~~happen~~ occur. ~~But~~ However, because of the frequent output of the auxiliary pulse, power consumption rises and remaining operation time is shortened~~s~~. This kind of quality problem ~~cannot~~ could previously not be properly discovered until now due to no time delay being observed, but ~~the~~ mode 3 makes the detection certain.

[0175] In the above embodiment, no special check equipment is necessary to conduct the operation check function. Therefore the present invention is easily applicable to ~~the~~ cases of, for example, advancing to foreign market, or assembling at several regions or places. And even after the shipment for example at the store or at the sales department or the like, it is possible to verify the timepiece operation easily.

[0176] Methods corresponding to the modes 1 to 3 mentioned above can be ~~solely~~ individually used. ~~, f~~For example the following utilizations are possible.

[0177] Manufacturing and using battery voltage adjusting devices corresponding to the mode 1.

[0178] Manufacturing and using check devices or full-charge notification devices corresponding to the mode 2.

[0179] Manufacturing check devices corresponding to both of the mode 1 and 2, and using them for checking of generation unit of analog, digital, or analog-digital combination ~~electrical~~electric timepieces.

[0180] Configuring operation check system corresponding to all of the mode 1, 2, and 3, and using them for operation checking of analog, digital, or analog-digital combination ~~electrical~~electric timepieces.

[0181] Combining the modes 1 and 3, and using for various devices.

[0182] Combining the modes 2 and 3, and using for various devices.

[0183] Also, in the above embodiment, the operation result of each mode (states of discharging or charging or operation check result) is revealed by changing the displaying state (hand movement state) on the time displaying section. But this is not limited to the above form, and other method can be used to reveal the operation result of each mode. For example, if the timepiece has a digital displaying section, it is possible to change the displaying state from the non-displaying state to other state, and thus to enable the notification of the operation result. And if the

timepiece has a sound wave generating element or display light, by shifting of sound generation and sound non-generation, by turning the light on/off, by shifting of the sound generation state (frequency, generation cycle, or the like), or by changing the flashing period of the display light, it is possible to notify the charging state or the check result.

[0184] The embodiment of the present invention is not limited to the above embodiment. For example, the charging device for the battery is not limited to the provision as an internal unit, but can be provided as a removable unit or as an external unit.

[0185] In the above embodiment, a timepiece is exemplified with a generator of an oscillating weight or the like is driven by kinetic energy and the electricity is generated by the rotation from the oscillation weight and then by the electricity the timepiece works. But the present invention is not limited to this. Other generation methods ~~is~~ are also possible for an ~~electrical~~electric timepiece such as ~~seizing~~ using light energy ~~with~~ from a solar panel, such as ~~seizing~~ thermal energy with a Peltier element, and such as ~~seizing~~ using strain energy ~~with~~ from a piezo element. Other method is also possible for an ~~electrical~~electric timepiece by providing electricity generated by an electromagnetic induction from outside of the timepiece, and then a stepping motor is moved by the electricity. In addition to timepieces, the present invention is applicable to stopwatches and other time keeping apparatus. And the raising and lowering circuit 49 can be omitted. In that case, the circuit driven by the output voltage VSS of the circuit 49 is driven by the output voltage VTKN of the battery 48.